WHAT IS CLAIMED IS:

1. A semiconductor circuit comprising:

a first transistor having:

a first bulk;

spaced-apart source and drain regions formed in the first bulk;

a first channel defined between the source and drain regions, the first channel having a first channel length and a first dopant concentration;

a layer of first gate oxide formed over the first channel, the layer of first gate oxide having a thickness; and

a gate formed over the layer of first gate oxide;

the first transistor conducting more than a leakage current when the gate, the source, and the bulk are connected to a same potential; and

a second transistor having:

a second bulk;

spaced-apart source and drain regions formed in the second bulk;

a second channel defined between the source and drain regions formed in the second bulk;

a layer of second gate oxide formed over the second channel, the second channel having a second channel length and a second dopant concentration, the layer of second gate oxide having a thickness, and

a gate formed over the layer of second gate oxide;

the second transistor being substantially non-conductive when the gate, the source, and the second bulk are connected to a same potential, the first channel having a first channel length approximately 0.3 to 0.8 as long as the second channel length.

2. The circuit of claim 1 wherein the thickness of the layer of first gate oxide is substantially equal to the thickness of the layer of second gate oxide.

3. The circuit of claim 2 wherein the first dopant concentration is greater than the second dopant concentration.

4. The circuit of claim 2 and further comprising a third transistor formed in the semiconductor material, the third transistor having a third channel and a layer of third gate oxide formed over the third channel, the third channel having a third channel length and a third dopant concentration, the layer of third gate oxide having a thickness, the third transistor being substantially non-conductive when zero volts are applied to the gate, the thickness of the layer of third gate oxide being greater than the thickness of the layer of second gate oxide.

5. The circuit of claim 4 wherein the first dopant concentration is substantially equal to the second dopant concentration and the third dopant concentration.

6. The circuit of claim 5 wherein the second and third transistors have source and drain regions of the same conductivity type,

and the first transistor has source and drain regions of an opposite conductivity type.

7. The circuit of claim 6 wherein the first and second transistors have source and drain regions of the same conductivity type, and the third transistor has source and drain regions of an opposite conductivity type.

8. The circuit of claim 1 wherein the thickness of the layer of first gate oxide is substantially less than the thickness of the layer of second gate oxide.

9. The circuit of claim 8 wherein the first dopant concentration is greater than the second dopant concentration.

10. The circuit of claim 8 and further comprising a third transistor formed in the semiconductor material, the third transistor having a third channel and a layer of third gate oxide formed over the third channel, the third channel having a third channel length and a third dopant concentration, the layer of third gate oxide having a thickness, the third transistor being substantially non-conductive when zero volts are applied to the gate, the thickness of the layer of third gate oxide being substantially equal to the thickness of the layer of first gate oxide.

11. The circuit of claim 10 wherein the first dopant concentration is substantially equal to the second dopant concentration and the third dopant concentration.

12. The circuit of claim 11 wherein the second and third transistors have source and drain regions of the same conductivity type, and the first transistor has source and drain regions of an opposite conductivity type.

13. The circuit of claim 12 wherein the first and third transistors have source and drain regions of the same conductivity type, and the second transistor has source and drain regions of an opposite conductivity type.

14. The circuit of claim 1 and further comprising a well, only the first transistor being formed in the well.

15. A method for forming a semiconductor circuit in a semiconductor material of a first conductivity type, the semiconductor circuit having a first channel region, a second channel region, and a third channel region, the method comprising the steps of:

implanting the first channel region and the second channel region to add a channel dopant concentration to the first channel region and a channel dopant concentration to the second channel region, the first and second channel dopant concentrations being substantially equal;

forming a layer of first oxide on the first channel region and a layer of second oxide on the second channel region;

forming a layer of first polysilicon on the layer of first oxide and a layer of second polysilicon on the layer of second oxide; and

etching the layer of first polysilicon to form a first gate on the first region and the layer of second polysilicon to form a second gate on the second region, the first gate having a length 0.3 to 0.8 as long as a length of the second gate.

16. The method of claim 15 wherein a thickness of the layer of first oxide is substantially equal to a thickness of the layer of second oxide.

17. The method of claim 16 and further comprising the steps of:

implanting the first channel region and the third channel region to add a region dopant concentration to the first channel region and a region dopant concentration to the third channel region, a dopant concentration in the first channel region being equal to the channel dopant concentration and the region dopant concentration, a dopant concentration in the second channel region being equal to the channel dopant concentration, and a dopant concentration in the third channel region being equal to the region dopant concentration;

forming a layer of third oxide on the third channel region, the layer of third oxide being thicker than the layer of second oxide;

forming a layer of third polysilicon on the layer of third oxide; and

etching the layer of third polysilicon to form a third gate on the third region.

18. The method of claim 17 and further comprising the steps of:

implanting the first channel region, the third channel region, and a fourth channel region to add a blanket dopant concentration to the first channel region, a blanket dopant concentration to the third channel region, and a blanket dopant concentration to the fourth channel region, a dopant concentration in the first channel region being equal to the channel dopant concentration, the region dopant concentration, and the blanket dopant concentration, a dopant concentration in the second channel region being equal to the channel dopant concentration and the blanket dopant concentration, a dopant concentration in the third channel region being equal to the region dopant concentration, and a dopant concentration in the fourth channel region being equal to the blanket dopant concentration;

forming a layer of fourth oxide on the fourth channel region, the layer of third oxide being thicker than the layer of fourth oxide;

forming a layer of fourth polysilicon on the layer of fourth oxide; and

etching the layer of fourth polysilicon to form a fourth gate on the fourth region.